That is, the second conducive ring **326** may extend along the second row Row2. Although only a part of the second conductive ring **326** is illustrated, the second conductive ring **326** may be disposed to form a closed curve inside the semiconductor chip. The second conductive ring **326** may be connected to the second pad **322** through internal interconnection lines (not illustrated).

[0105] According to the example embodiments, instead of providing a separate input/output unit to include pads receiving a power supply voltage, a pad that receives a power supply voltage may be disposed in an input/output unit in which a pad that receives a ground voltage is disposed. For example, referring to FIG. **12**, the second additional pad **322**A is disposed in the fifth input/output unit (I/O Unit_5) separately provided to receive a ground voltage. That is, instead of providing a separate input/output unit to receive a power supply voltage, the second additional pad **322**A may be disposed inside the fifth input/output unit (I/O Unit_5) in which a pad that receives a ground voltage is disposed. An SSN of a signal being input through the third pad **332** may be reduced by disposing the first pad **312** and the second additional pad **322**A in one input/output unit. Also, a size of the semiconductor chip may be reduced.

[0106] FIG. **13** is a top plan view illustrating a part of a semiconductor chip in accordance with example embodiments. FIG. **14**A is a cross-sectional view taken along the line A-A' of FIG. **13**. FIG. **14**B is a cross-sectional view taken along the line B-B' of FIG. **13**. FIG. **14**C is a cross-sectional view taken along the line C-C' of FIG. **13**. FIG. **15**A is a cross-sectional view taken along the line D-D' of FIG. **13**. FIG. **15**B is a cross-sectional view taken along the line E-E' of FIG. **13**. FIG. **15**C is a cross-sectional view taken along the line F-F' of FIG. **13**.

[0107] Referring to FIGS. **13** through **15**C, first pads **312** may be disposed along a first row Row1. A first conductive ring **316** may be disposed inside a semiconductor chip **300** under the first pads **312**. The first pads **312** may be connected to the first conductive ring **316** through first internal interconnection lines **314**. The first conductive ring **316** may be disposed inside the semiconductor chip **300** at a depth of h1. As illustrated in FIG. **14**A, the first pads **312** may be connected to the first conductive ring **316** to have a minimum distance therebetween. That is, each of the first pads **312** may be connected to the first conductive ring **316** to have a length of h1 therebetween.

[0108] Second pads **322** may be disposed along a second row Row2. A second conductive ring **326** may be disposed inside the semiconductor chip **300** under the second pads **322**. The second pads **322** may be connected to the second conductive ring **326** through second internal interconnection lines **324**. The second conductive ring **326** may be disposed inside the semiconductor chip **300** to a depth of h2. As illustrated in FIG. **14**B, the second pads **322** may be connected to the second conductive ring **326** to have a minimum distance therebetween. That is, each of the second pads **322** may be connected to the second conductive ring **326** to have a length of h2 therebetween.

[0109] In this case, some of the second pads (or second additional pads **322**A) may be disposed along a third row Row3. A second additional internal interconnection line **324**A may connect the second additional pad **322**A to the second conductive ring **326**. As illustrated in FIG. **15**B, the second additional internal interconnection line **324**A may be disposed in the form of an "L" character.

[0110] Third pads **332** may be disposed along the third row Row3. Third internal interconnection lines (not illustrated) may connect the third pads **332** to a logical circuit (not illustrated) and a signal input through the third pads **332** may be transmitted to the logical circuit through the third internal interconnection lines.

[0111] FIG. **16** is a drawing illustrating a part of FIG. **13** in three dimensions.

[0112] Referring to FIG. **16**, the first pads **312** is disposed along the first row Row1 and the first conductive ring **316** is disposed inside the semiconductor chip **300** under the first pad **312**. The first pad **312** is connected to the first conductive ring **316** to have a minimum distance therebetween through the first internal interconnection line **314**.

[0113] Although not shown in FIG. **16**, the second pads may be disposed along the second row and the second conductive ring may be disposed inside the semiconductor chip **300** under the second pad. The second pad and the second conductive ring may be connected to each other by the second internal interconnection line to have a minimum distance therebetween.

[0114] The second additional pad **322**A is disposed on the third row Row3. The second additional pad **322**A is connected to the second conductive ring **326** by a second additional internal interconnection line **324**A having an "L" character shape. A shape of the second additional internal interconnection line **324**A is not limited to the "L" character and the second additional internal interconnection line **324**A may have various shapes.

[0115] Although not shown in FIG. **16**, the third pads may be disposed along the third row Row3 and the third pads may be connected to a logical circuit (not illustrated) through the third internal interconnection lines.

[0116] The first pad **312** disposed on the first row Row1 is connected to the first conductive ring **316**, and the second additional pad **322**A disposed on the third row Row3 is connected to the second conductive ring **326**. The first conductive ring **316** and the second conductive ring **326** may be connected to an ESD circuit (not illustrated) disposed inside the semiconductor chip **300**. The ESD circuit may be connected to the logical circuit disposed inside the semiconductor chip **300** to stably supply a power supply voltage to the logical circuit. The third pads may be connected to the logical circuit disposed inside the semiconductor chip **300** by the third internal interconnection lines.

[0117] According to the example embodiments, instead of providing a separate input/output unit to supply a power supply voltage, the second additional pad **322**A may be disposed in an input/output unit (e.g., I/O Unit_5) where the first pad **312** for supplying a ground voltage is disposed. That is, since a power supply voltage can be sufficiently supplied without providing a separate input/output unit for supplying a supply voltage, an SSN of a signal being input through the third pad **332** may be reduced. Additionally, since a separate input/output unit for supplying a ground voltage and a power supply voltage is omitted, a chip size may be reduced.

[0118] According to the example embodiments, a method of disposing pads of a semiconductor chip capable of stably supplying a power supply voltage may be provided.

[0119] According to the example embodiments, a method of disposing pads of a semiconductor chip capable of reducing a chip size may be provided.